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EXAMINER	
PATEL, PARESH H	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 06/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/804,582	FRANKOWSKY ET AL.	
	Examiner	Art Unit	
	Paresh Patel	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-14,16-20 and 23-275* is/are rejected.

7)☒ Claim(s) *6,15,21-22,26,28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed on 02/27/2006 have been fully considered but they are not persuasive. With respect to claim 1, Applicant argues Schnabel reference discloses that the test terminals are always connected to the memory 2 and therefore switching device is not selectively couple as claimed. Examiner respectfully disagrees because during testing switching device selectively connects the test terminal to the voltage line (not shown because it is inherent) of the memory 2. Also, an internal voltage line as argued here is inherent to the memory 2, because ordinary skill in the art knows that memory will only function with application of voltage, and internal wires that carries these voltage are the claimed internal voltage line. Since, claimed voltage line receives signal voltage during testing of the first circuit it reads on the memory 2 of Schnabel reference. Regarding claim 23, Applicants argument about constant electrical connection is not true because switch is activated during testing as further claimed. About Van Brunt reference, Applicants argues Van Brunt does not disclose the internal voltage lines which are connected to the test terminal. Examiner disagrees with Applicants for the same reason as mentioned in the office action of 12/27/2006.

Claim Objections

2. Claim 6 is objected to because of the following informalities: at last lines 2-3 "line the internal voltage supply is" should read -- line, the internal voltage line is--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 6 and 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: between the test device and the internal voltage supply as claimed, since last line is unclear.

Regarding claim 10, it is not clear how the switch device is further configured to isolate the test terminal from the test circuit, while the switch device is coupled to an output of the test circuit (see claim 7).

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-5, 7-9 and 13-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Koshikawa (US 5428299).

Regarding claim 1, Koshikawa in fig. 5 discloses an integrated circuit [21], comprising:

a first circuit [26 (i.e. first and second voltage generating circuit) with 22] to be tested circuit comprising an internal voltage line [Vint];

a test circuit [23] for testing the first circuit;

a test terminal [Pext] coupled to the test circuit in order to provide an activation signal activating the test circuit to perform a test function; and

a switching device [24] to selectively couple the test terminal to the internal voltage line during testing of the test circuit [lines 55-68 of column 8 and fig. 6].

Regarding claim 2, Koshikawa discloses the integrated circuit of claim 1, wherein the test terminal is coupled to the internal voltage line to provide an electrical signal to the internal voltage line from an external source [Vext].

Regarding claim 3, Koshikawa discloses the integrated circuit of claim 1, wherein the switching device is further configured to isolate the test terminal from the test circuit after the activation of the test circuit [i.e. at Vext is lower, lines 3-12 of column 9].

Regarding claim 4, Koshikawa discloses the integrated circuit of claim 1, wherein the first circuit further comprises an internal voltage supply [step-down voltage generator 26].

Regarding claim 5, Koshikawa discloses the integrated circuit of claim 4, further comprising another switching device [25] responsive to the switching signal [EBL1] to selectively couple the internal voltage supply to the internal voltage line.

Regarding claim 7, Koshikawa discloses an integrated circuit [21], comprising:

a first circuit [26 and 22] to be tested comprising an internal voltage line [Vint];

a test circuit [23] for testing the useful circuit;

a test terminal [Pext] coupled to the test circuit in order to provide an activation signal activating the test circuit to perform a test function; and

a switching device [25a] coupled to an output of the test circuit and configured to selectively couple the test terminal to the internal voltage line in response to a switching signal from the output [VR].

Regarding claim 8, Koshikawa discloses the integrated circuit of claim 7, wherein the test circuit is configured to output the switching signal in response to receiving the activation signal [Vext].

Regarding claim 9, Koshikawa discloses the integrated circuit of claim 7, wherein the test terminal is coupled to the internal voltage line to provide an electrical signal to the internal voltage line from an external source [Vext].

Regarding claim 13, Koshikawa discloses the integrated circuit of claim 7, wherein the first circuit further comprises an internal voltage supply [26].

Regarding claim 14, Koshikawa discloses the integrated circuit of claim 13, further comprising another switching device [25b] responsive to the switching signal to selectively couple the internal voltage supply to the internal voltage line.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-3 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Schnabel (US 6788087).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claims 1 and 23 Schnabel in fig.1-2 discloses an integrated circuit [1], comprising:

a first circuit [2] to be tested comprising an internal voltage line [voltage line of 2];

a test circuit [3] for testing the first circuit;

a test terminal [5] coupled to the test circuit in order to provide an activation signal activating the test circuit to perform a test function [via 8] ; and

a switching device [11, 12 and 8] to selectively couple the test terminal to the internal voltage line during testing of the first circuit.

Regarding claim 2, Schnabel discloses the test terminal is coupled to the internal voltage line to provide an electrical signal to the internal voltage line from an external source [22].

Regarding claim 3, Schnabel discloses the switching device is further configured to isolate the test terminal from the test circuit after the activation of the test circuit [see Abstract].

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 7-11, 12, 16-19, 23-25 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Brunt (US 4357703) in view of Tada et al. (US 4801871).

Regarding claims 7, 9, 16 and 23-24, Van Brunt (hereafter Van) discloses a test system [fig. 1] for testing an integrated circuit, comprising:

a first circuit [11] to be tested comprising an internal voltage line;

a test circuit [40, 20, 22] for testing the first circuit;

a test terminal [21] coupled to the test circuit in order to provide an activation signal activating the test circuit to perform a test function [test data input];

a switching device [23] coupled to an output of the test circuit and configured to selectively couple [using 40] the test terminal to the internal voltage line [of 11] in response to a switching signal from the output.

Van discloses all the elements including an external test device [lines 1-3 of column 4] connected to the integrated circuit via the test terminal. Van is silent about said external test device comprising (i) a test module for issuing the activation signal; and (ii) a power supply for providing an electrical signal to the internal voltage line after the activation of the test circuit.

Tada et al. (hereafter Tada) in fig. 1 and 4 discloses the external test device [30] comprising (i) a test module [D and C] for issuing the activation signal; and (ii) a power supply [PS, GND] for providing an electrical signal to the internal voltage line after the activation of the test circuit [1].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to replace tester of Van with tester as taught by Tada, in order to test circuits without changing wiring boards and to reduce testing cost.

Regarding claim 17, Tada discloses (in fig. 4) the external test device further comprises an external test device switch [programmable R1, R2, RV and RG] for selectively coupling the test module and power supply to the test terminal.

Regarding claims 8, 18 and 25, Van discloses the test circuit is configured to output the switching signal in response to receiving the activation signal.

Regarding claims 10, 19 and 27, Van discloses the switching device is further configured to isolate the test terminal from the test circuit after the activation of the test circuit.

Regarding claim 12, Van discloses the test circuit is configured to deactivate as claimed.

Regarding Claim 11, the combination of Van and Tada discloses all the elements except for test circuit comprise a memory element to store activation information. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use memory element as claimed for storing the information, since it was known in the art to store the information for programming including control application.

11. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schnabel as applied to claim 1 above, and further in view of Horiguchi et al. (US 5347492).

Regarding claim 4, Schnabel discloses all the elements except for the first circuit further comprise an internal voltage supply. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use internal voltage supply to operate partial circuit, since it was known in the art to reduce the power consumption of the integrated circuit [see lines 15-21 of column 1, US 5347492].

12. Claims 13 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van and Tada as applied to claims 7 and 16 above, and further in view of Horiguchi et al. (US 5347492).

Regarding claims 13 and 20, the combination of Van and Tada discloses all the elements except for the first circuit further comprise an internal voltage supply. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use internal voltage supply to operate partial circuit, since it was known in the art to reduce the power consumption of the integrated circuit [see lines 15-21 of column 1, US 5347492].

Allowable Subject Matter

13. Claims 6, 15, 21-22, 26 and 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. See office action dated 09/15/2005 for reason for allowance.

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paresh Patel whose telephone number is 571-272-1968. The examiner can normally be reached on 8:00 to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on 571-272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Paresh Patel
Primary Examiner
Art Unit 2829

June 08, 2006